CLAIMS

What is claimed is:

1. A processor, comprising;

a plurality of registers, wherein each of the plurality of registers comprises data bits for holding data and one or more flag and status bits for holding carry flag information;

an arithmetic logic unit, the arithmetic logic unit coupled to the plurality of registers, wherein the arithmetic logic unit is configured to write data and carry flag information to one of the plurality of registers.

2. The processor of claim 1, wherein the one or more flag and status bits hold overflow flag information.

3. The processor of claim 2, wherein the one or more flag bits hold sticky overflow flag information.

4. The processor of claim 1, wherein the processor is a multithreaded processor.

5. The processor of claim 1, wherein providing flag and status information in each of the plurality of registers allows the processor to handle a plurality of threads, wherein each thread uses writes disparate flag and status bits.

6. The processor of claim 5, wherein the plurality of threads are each associated with a subset of the plurality of registers.

7. The processor of claim 6, further comprising context circuitry associated with the plurality of threads, wherein the context circuitry is operable to track which of the plurality of threads is being processed by a particular stage.

8. The processor of claim 6, wherein the arithmetic logic unit is operable to process the plurality of threads, the arithmetic logic unit configured to process a particular thread for a single clock cycle before context switching to process a next thread, wherein each of the plurality of threads are processed for the single clock cycle before context switching.

9. The processor of claim 1, wherein the processor is a processor core on a programmable chip.

10. The processor of claim 8, wherein the particular thread is processed for a single clock cycle to allow a memory access to complete before continuing processing of the particular thread.

11. The processor of claim 10, wherein the program counters track the processing location of each thread.

12. The processor of claim 1, wherein the plurality of registers are configured as memory on a programmable chip.

13. The processor of claim 1, wherein the processor is a central processing unit or a digital signal processor.

14. The processor of claim 1, wherein context circuitry is a context register.

15. The processor of claim 14, wherein the processor comprises a plurality of stages, each stage having an associated context register.

16. The processor of claim 15, wherein each thread is associated with a program counter.

17. The processor of claim 16, wherein the plurality of stages comprise reading the context register, accessing the program counter, obtaining an instruction, decoding the instruction, executing the operation, and writing a result to one of the plurality of registers.

18. The processor of claim 10, further comprising a plurality of program counters associated with the plurality of threads.

19. A method for processing data, comprising;

providing data to an arithmetic logic unit associated with a processor, the data obtained from registers comprising data bits for holding data and one or more flag and status bits for holding carry flag information;

processing the data at the arithmetic logic unit, the arithmetic logic unit coupled to the plurality of registers, wherein the arithmetic logic unit is configured to write data and carry flag information to a result register.

20. The method of claim 19, wherein the one or more flag and status bits hold overflow flag information.

21. The method of claim 20, wherein the one or more flag bits hold sticky overflow flag information.

22. The method of claim 19, wherein the processor is a multithreaded processor.

23. The method of claim 19, wherein providing flag and status information in each of the plurality of registers allows the processor to handle a plurality of threads, wherein each thread uses writes disparate flag and status bits.

24. The method of claim 23, wherein the plurality of threads are each associated with a subset of the plurality of registers.

25. The method of claim 24, further comprising context circuitry associated with the plurality of threads, wherein the context circuitry is operable to track which of the plurality of threads is being processed by a particular stage.

26. The method of claim 25, wherein the arithmetic logic unit is operable to process the plurality of threads, the arithmetic logic unit configured to process a particular thread for a single clock cycle before context switching to process a next thread, wherein each of the plurality of threads are processed for the single clock cycle before context switching.

27. A programmable chip, comprising;

means for providing data to an arithmetic logic unit associated with a processor on the programmable chip, the data obtained from registers comprising data bits for holding data and one or more flag and status bits for holding carry flag information;

processing the data at the arithmetic logic unit, the arithmetic logic unit coupled to the plurality of registers, wherein the arithmetic logic unit is configured to write data and carry flag information to a result register.

28. The programmable chip of claim 27, wherein the one or more flag and status bits hold overflow flag information.

29. The programmable chip of claim 28, wherein the one or more flag bits hold sticky overflow flag information.

30. The programmable chip of claim 27, wherein the processor is a multithreaded processor.

31. The programmable chip of claim 27, wherein providing flag and status information in each of the plurality of registers allows the processor to handle a plurality of threads, wherein each thread uses writes disparate flag and status bits.